A HIGH EFFICIENCY COMPLEMENTARY GaAs POWER FET TECHNOLOGY FOR SINGLE SUPPLY PORTABLE APPLICATIONS

Elizabeth Glass, Jon Abrokwah, Rudy Lucero, Eddie Spears*, Jeff Rollman, Jenn-Hwa Huang, Bruce Bernhardt* and Bill Ooms**

Phoenix Corporate Research Laboratories
Motorola, Inc.

2100 E. Elliot Rd, MD-EL508, Tempe, AZ 85284
*** Communications Product Laboratory, Tempe, AZ**
****Land Mobile Products Sector, Plantation, FL**

ABSTRACT

A high efficiency enhancement mode power heterostructure FET has been developed for single supply portable applications. The device requires only a single 3V supply for operation, making it an ideal candidate for portable applications. At 850 MHz, a 1.0 μm x 12 mm N-type FET exhibited a power output of +30.7 dBm, power gain of 10.6 dB, and a power-added efficiency of 60%, at a drain to source voltage of 3V, and drain to source quiescent current of 150 mA. This device was fabricated on a standard Complementary GaAs (CGaAs™) process flow, which is capable of simultaneously building low-voltage, low-power digital circuits (200MHz), high-speed digital circuits (5 GHz), and RF power circuits (900 MHz).

INTRODUCTION

GaAs FETs are increasingly used in portable communication transmitters because of their superior efficiencies at lower drain voltages (less than 4.0 V). Driver amplifiers and output power amplifiers incorporating GaAs MESFETs and HFETs have been reported. To date, depletion mode devices have been the only type of device with adequate efficiency performance for increasingly demanding power amplifier applications. In order to bias these normally-on devices to the desired level, a negative voltage is applied from the gate to source terminal. Additional circuitry must be included on-board to generate this regulated negative voltage, resulting in increased size, cost and current drain.

The N-type FET in the CGaAs™ (Complementary heterostructure GaAs) process is an enhancement mode device with a high gate turn-on voltage, typically 1.5 V, providing large voltage swing and a good drive current. It requires only a single positive voltage supply for its operation. This normally-off characteristic makes it an attractive candidate for use in portable RF circuit applications. By eliminating the negative voltage supply, the component count and circuit complexity in today's portable communication products can be greatly reduced. In addition, the noise

0-7803-3360-8/96/$5.00 © IEEE

associated with generating a negative voltage is eliminated. The importance of this is illustrated by the recent increase in papers on single supply devices and amplifiers [1] [2]. This paper reports on CGaAs N-type FET's that were fabricated in Motorola's CS-1 fabrication facility. The RF characteristics of these single supply enhancement mode devices are explored and the results are believed to be the best reported to date.

DEVICE & PROCESSING

The manufacturable CGaAs process used to fabricate this device has been reported earlier [3] [4]. A schematic cross-section of the epitaxial material structure and the self-aligned ion-implanted NFET process is shown in Figure 1. The structure consists of a 30Å GaAs cap, 250Å of undoped $Al_{0.75}Ga_{0.25}As$, 150Å undoped $In_{0.2}Ga_{0.8}As$, and 2000Å undoped GaAs buffer/LEC GaAs. The 30Å undoped GaAs cap protects the high mole fraction AlGaAs from surface oxidation. The silicon delta doping is 30Å away from the InGaAs/GaAs interface and controls the threshold voltage. The gate metal is 4000Å of RF reactively sputtered TiWN. The implants are self-aligned to the refractory gates. The devices are isolated by oxygen implantation and have refractory ohmic contacts. Devices are passivated with SiO_2 and Si_3N_4. The interconnect metal process is the same as that of Motorola's GaAs E/D MESFET process.

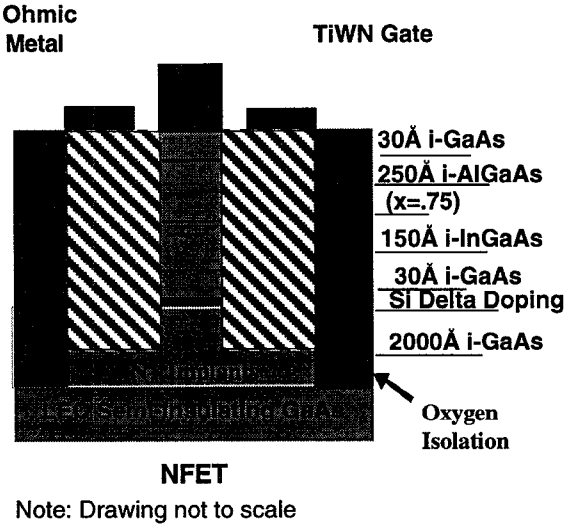

Fig. 1. Cross sectional view of the enhancement mode HFET structure.

Although developed for digital applications, examination of the N-type device DC characteristics suggested that an investigation of the RF characteristics was warranted. 1 µm x 12 mm N-type devices were statistically characterized across a wafer for DC performance. G_m, ID_{max}, BV_{gdo}, and subthreshold current were measured. The mean g_m was 180 mS/mm at V_{ds} = 3V. The mean threshold voltage (Vth) was +0.5V with a mean turn-on voltage (V_{to}) of +1.6V, yielding a total potential RF gate swing of 1.1V before gate-source diode turn-on. The mean sub-threshold leakage current for V_{ds} = 3V and V_{gs} = 0V was less than 1 µA. The mean gate to drain breakdown voltage was 6V as measured at Ig = 12mA.

RESULTS

Smaller devices, 1.0 µm x 3mm, were on-wafer probed and characterized for small signal performance using an HP8510 network analyzer. At 850 MHz, the FET exhibited a M.A.G. of 23 dB. 1.0 µm x 12mm devices were soldered into evaluation packages and characterized on a Maury semi-automated load pull system. The FET was biased at V_{ds} = +3V and V_{gs} = +0.7V with a quiescent current of I_{ds} = 150 mA. Load and source impedances were found that produced a reasonable compromise between output power and power added

efficiency. Figure 2 shows the resultant RF power performance of the device. At a +20dBm input power the output power was +30.7 dBm, the P.A.E. was 60%, and the corresponding gain was 10.6 dB.

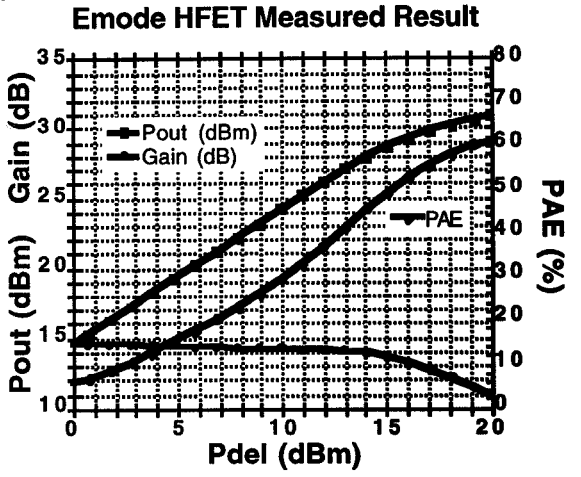

Fig. 2 Swept power measurement of an enhancement mode HFET at 850 MHz at 3V.

12mm devices were then designed into hybrid amplifiers and their performance was evaluated over temperature and voltage extremes. Power output and power added efficiency were measured from +25°C to +100°C. The performance is shown in Figure 3. After one hour of continuous operation, the power slump for the amplifier was -1.85 dB, which is well below specification for many portable applications. The hybrid amplifiers were operated into a 20:1 VSWR at 100 °C and at a drain voltage exceeding 6V before experiencing device performance degradation.

The device drain to source leakage current in the "off" state (V_{GS}=0V) is an important performance parameter for portable products operating under strict current budgets. Low leakage current performance allows the elimination of supply switches which will make systems less expensive and more efficient. Figure 4 shows the maximum "off" state leakage current over temperature extremes is less than or equal to 2 µA. This value is below the self-discharge rate of a NiCd battery that is typically used to power portable products.

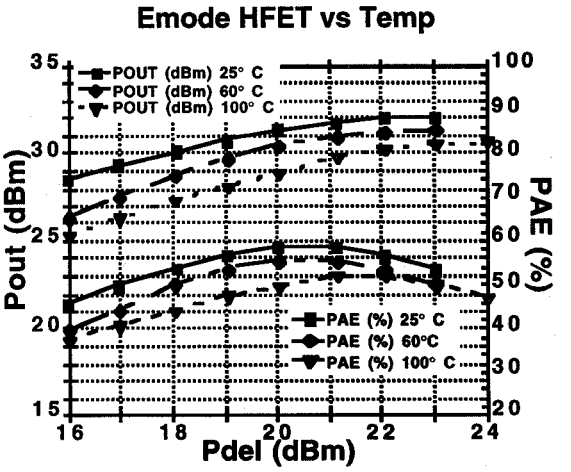

Fig 3. Measured Power Output, PAE and Gain of enhancement mode HFET at 3.0 V from +25° C to +100° C.

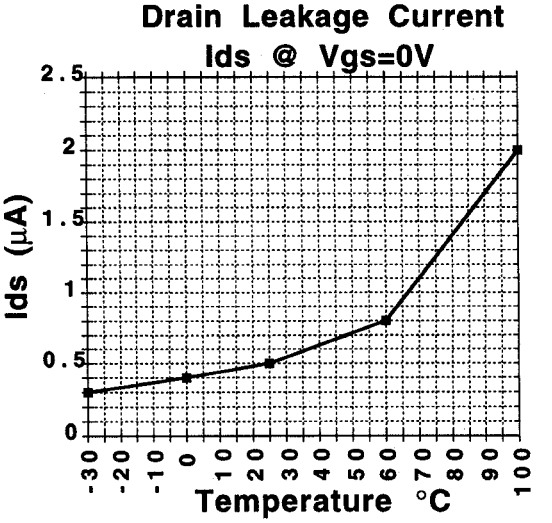

Fig 4. Measured drain to source leakage current at Vgs=0V and Vds=3.0 V from +25° C to +100° C.

The devices also exhibited excellent stability over temperature and voltage extremes. The only non-harmonic spurious response noted was into a 20:1 VSWR at ±100 MHz from the carrier at one phase angle.

CONCLUSIONS

A high efficiency enhancement mode power heterostructure FET has been designed, fabricated and tested for application as a single supply power amplifier for wireless communication systems. At 850 MHz, a power added efficiency of 60 % and an output power of +30.7 dBm at 10.6 dB gain was achieved at V_{ds}=3.0.

ACKNOWLEDGMENTS

The authors would like to thank the CS-1 production facility personnel for fabrication of the devices. CGaAs™ is a trademark of Motorola Inc.

References

[1] M. Nagaoka, T. Inoue, K. Kawakyu, S. Obayashi, H. Kayano, E. Takagi, Y. Tanabe, M. Yoshimura, K. Ishida, Y. Kitaura and N. Uchitomi, "High-Efficiency Monolithic GaAs Power MESFET Amplifier Operating With A Single Low Voltage Supply for 1.9 GHz Digital Mobile Communication Applications", MTT-S International Microwave Symposium Digest, Vol. 2, pp. 577 - 580, 1994.

[2] S. Nakajima, K-I Matsuzaki, K. Otobe, H. Nishizawa, and N. Shiga, "Enhancement-Mode GaAs MESFET technology for low consumption power and low noise applications," IEEE Trans. Microwave Theory and Technique Symposium Technical Digest., pp. 1443-1446, 1994.

[3] B. Bernhardt, M. LaMacchia, J. Abrokwah, J. Hallmark, R. Lucero, B. Mathes, B. Crawforth, D. Foster, K. Clauss, S. Emmert, T. Lien, E. Lopez, V. Mazzotta, B. Ooms, "Complementary GaAs (CGaAs™): A High Performance BiCMOS Alternative", GaAs IC Symposium Technical Digest, pp. 18-21, 1995.

[4] J. Hallmark, C. Shurboff, W. Ooms, R. Lucero, J. Abrokwah, and J. Huang, "0.9V DSP Blocks, A 15ns 4K SRAM and a 45ns 16-bit Multiply/Accumulator," 1994 IEEE GaAs IC Symposium Technical Digest, pp. 55.